SEMICONDUCTOR MEMORY WITH ALTERNATELY MULTIPLEXED ROW AND COLUMN ADDRESSING

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

BACKGROUND OF THE INVENTION

This invention relates to a semiconductor memory, such as a dynamic RAM, for example.

Conventional semiconductor memories, such as dynamic RAMs, are based on the input multiplexing of the row address and column address, and they necessitate a row address strobe, column address strobe and several other timing signals including write control signals, as is well known in the art.

A computer system generally operates in synchronism with a constant system clock, and data to be read out or written into a storage unit is transferred also in synchronism with the system clock. Accordingly, for a storage unit based on the dynamic RAM, in which several timing signals are produced from the system clock, these timing signals need to be set to meet the prescribed timings even in the worst condition in consideration of the variability in the signal delay time, crosstalk noise, and the like. On this account, conventional semiconductor memories cannot fully exert their inherent performances.

SUMMARY OF THE INVENTION

An object of this invention is to provide a semiconductor memory, e.g., a dynamic RAM, which operates with its full performance.

The inventive address-multiplexed semiconductor memory is designed to receive a clock signal and a chip select signal from the outside and have its memory cell array access controlled based on the clock signal. Consequently, by supplying an external clock signal which meets the performance of the semiconductor memory, it can operate with its full performance.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of the semiconductor memory according to an embodiment of this invention;

FIGS. **2A** and **2B** are timing charts used to explain the operation of the arrangement shown in FIG. **1**;

FIG. **3** is a diagram showing the control circuit and its periphery in FIG. **1**; and

FIGS. **4**, **5** and **6** are timing charts used to explain the operation of the arrangement shown in FIG. **3**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A specific embodiment of this invention will be described with reference to the drawings.

In FIG. **1**, a system clock CLK, which is produced inside a computer system, is supplied from the outside of the semiconductor memory, and it is delivered to the clock input terminals of latches **81–84** in a latch circuit **8** and the clock input terminal of a control circuit **1**. Also supplied from the outside are a chip select signal $\overline{CS}$, write enable signal $\overline{WE}$, and write data DIN, that are delivered to the latches **81–83** in the latch circuit **8** in synchronism with the system clock

CLK. The readout data DOUT from the latch **84** in the latch circuit **8** is delivered to the outside.

The control circuit **1** produces a row address set signal **RS1**, which is delivered to the set input terminal of a row latch **2**, which then introduces a row address multiplexed in the address signals **A0–A9**. Similarly, the column address set signal **CS1** is delivered to the set input terminal of a column latch **4**, which then introduces a column address multiplexed in the address signals **A0–A9**. Thus, the control circuit **1** and latches **2,4** demultiplex the address signals **A0–A9**.

The row latch **2** has its output signals delivered to the input terminals of a row decoder **3**, which produces output signals **X0–X1023** that are placed on the row lines (not shown) of a memory cell array **7**. The column latch **4** has its output signals delivered to the input terminals of a column decoder **5**, which produces output signals that are applied to the input terminals of a column selection circuit **6**. The column selection circuit **6** responds to the output signal of the column decoder **5** to select one of data input/output signals **Y0–Y1023** of the memory cell array **7**, so that the output of the latch **83** is written into a cell in write mode or data is read out to the latch **84** in read mode.

The operation of the foregoing arrangement will be explained on the timing charts of FIGS. **2A** and **2B**. FIG. **2A** shows the read cycle and write cycle, and FIG. **2B** shows reading and writing in the *page mode cycle, and the* refresh cycle **[**and page mode cycle**]**.

Read Cycle

The chip select signal $\overline{CS}$ is brought to a low level before the clock signal CLK first rises in its read cycle, and a row address RXi is applied to the address terminals **A0–A9**. The row address set signal **RS1** is produced at the first rising edge of the clock CLK, and the row address RXi is latched in the latch **2** shown in FIG. **1**. The row decoder **3** decodes the row address RXi which is latched in the row latch **2** thereby to activate a selected one of the row lines **X0–X1023**, and the read operation starts. Subsequently, a column address RYi is applied to the address terminals **A0–A9** before the second rise of the clock signal CLK of the READ cycle. Then, the column address set signal **CS1** is produced at the second rising edge of the clock signal CLK, and the column address RYi is latched in the column register **4** shown in FIG. **1**. The column decoder **5** decodes the column address RYi which is latched in the column latch **4**, and the column selection circuit **6** selects one of data read out to the data input/output signal lines **Y0–Y1023**. Subsequently, at the third rise of the clock signal CLK in the READ cycle, the data which has been selected by the column selection circuit **6** is latched in the latch **84** in the latch circuit **8**, and it is delivered as valid data at the terminal DOUT. The chip select signal $\overline{CS}$ is brought to a high level before third rise of the the clock signal CLK in the READ cycle, and the READ cycle operation for the memory cell array **7** completes at the fourth rise of the clock signal CLK.

Write Cycle

The operation until the rise of the first clock signal CLK is identical to the read cycle, and the explanation is omitted. The write enable signal $\overline{WE}$ is made low before the second rise of the clock signal CLK of the WRITE cycle, and write data is applied to the data input terminals DIN. The column address WYi is latched at the second rise of the clock signal CLK, and the write data at DIN terminal is latched in the latch **83** in the latch circuit **8**. The write data is transferred to one of the data input/output signal lines **Y0–Y1023**

selected with the column address WYi by the column selection circuit **6**, and it is written to the row line selected with the row address WXi.

Refresh Cycle

As in the read or write cycle, a refresh address RFi is latched in the row latch in response to the clock signal CLK of the first cycle and the row decoder **3** decodes the refresh address RFi latched in the latch **2** to activate *a* selected one of the row lines **X0–X1023**, and the refresh operation starts. Subsequently, the chip select signal $\overline{CS}$ is made high before the second clock signal CLK goes high. The chip select signal $\overline{CS}$ is disactivated when the second clock signal CLK rises, causing the column latch **4**, column decoder **5** and column selection circuit **6** to quit operation, and the data input/output operation does not take place. The clock signal CLK of the **[third]** *second* cycle is a dummy for making cycles consistent with the read and write cycle, and the refresh cycle completes by using clock signals CLK of three cycles.

Page Mode Cycle

The operations until the rise of the first and second rise of clock signal CLK are identical to the read or write cycle, and the explanation is omitted. In the third and following rises, reading or writing takes place in synchronism with the rising of the clock signal CLK for the row address (RXi or WXi respectively) and a column address (RY_K, RY_L or WY_K, WY_L respectively), which is different from the column address (RY_j or WY_j) entered in the first and second cycles. The page mode cycle continues until the chip select signal $\overline{CS}$ goes high. The figure shows the case in which row address RXi and column addresses RY_j, WY_K and WY_L are given in the respective first through fourth rises of the clock signal CLK.

FIG. **3** is a diagram showing the control circuit **1** and its periphery in FIG. **1**. In the figure, the chip select signal $\overline{CS}$ is applied to the data input terminal of the latch **81** in the latch circuit. The clock CLK is connected to the edge trigger T of the latch **81** the edge trigger T of the latch **10** in the control circuit **1** input terminal and delay circuit **12, 13**.

The output signal $\overline{CCS}$ of the latch **81** is delivered to the inverter **11**, which has an output CCS delivered to the data input terminal of latch **10** and input terminals of the two-input AND gate **14** and three-input AND gate **15**. The delay circuit **12, 13** has its output signal CLK1 applied to the input terminal of the three-input AND gate **15**.

The latch **10** has its output signal CT applied to the inverting input terminal of the two-input AND gate **14** and *to the input terminals of the* three-input AND gate **15**. The two-input AND gate **14** produces the row address set signal RS1 and the three-input AND gate **15** produces the column address set signal CS1.

The operation of the circuit arrangement shown in FIG. **3** will be explained for its read (write) cycle, refresh cycle and page mode read (or write) cycle, for example, on the timing charts of FIGS. **4, 5** and **6**.

In the read (or write) cycle of FIG. **4**, the chip select signal $\overline{CS}$ is made low before the clock signal CLK rises at t_1, and a low chip select signal $\overline{CS}$ is latched in the latch **81** at the rise of the clock signal CLK at t_1. At this time point t_1, the output signal $\overline{CCS}$ of the latch **81** is high. Because of a low data input signal CCS of the latch **10**, it latches the signal at the low level. The output signal CT of the latch **10** stays low until the rise of the next clock signal CLK at t_2. Because of a low input signal CCS of the two-input AND gate **14**, it produces a low output signal RS1 at t_1.

After the clock signal CLK has risen at t_1, the output signal $\overline{CCS}$ of the latch **81** goes low. Consequently, the output signal CCS of the inverter **11** goes high, causing the two-input AND gate **14** to output a low inverted input signal CT, and with high input signal CCS the AND gate **14** produces a high row address set signal RS1.

Next, when the clock signal CLK rises at t_2, the latch **10** has a high data input signal CCS and it latches the high-level signal. After the clock signal CLK has risen at t_2, the output signal CT of the latch **10** goes high. Because of inverting the high signal CT at the input of the two-input AND gate **14**, it produces a low output signal RS1. As the input signals CCS and CT of

the three-input AND gate **15** are high shortly after t_2, a clock signal CLK1 which is a delayed derivative of the clock signal CLK has its high-level portion between t_2 and t_3 delivered as a column address set signal CS1.

Through the foregoing operation, it becomes possible to introduce a row address and column address in the address signal **A0–A9** to the row latch **2** and column latch **4** sequentially.

Next, by making the chip select signal $\overline{CS}$ high before the clock signal CLK rises at t_3, a high-level signal is latched in the latch **81** at the rise of the clock signal CLK. After the clock signal CLK has risen at t_3, the output signal $\overline{CCS}$ of the latch **81** goes high. Accordingly, the signal CCS goes low, and the column address set signal CS1 produced by the three-input AND gate **15** goes low and stays low until the next rise of the clock signal CLK and lowering of the chip select signal CS.

Next, when the clock signal CLK rises at t_4, the signal CCS is low and the latch **10** latches the low-level signal to lower its output CT. After the clock signal CLK has risen at t_4, the output signal $\overline{CCS}$ of the latch **81** goes low. Because of a low output signal CT of the latch **10**, the two-input AND gate **14** produces a high row address set signal RS1 in response to the rise of its other input signal CCS.

The t_1 cycle and t_4 cycle have the same operation as described above, and it becomes possible to run the read (or write) cycles repeatedly.

FIG. **5** shows the refresh cycle. The cycle of t_1 is identical to that of t_1 of the read (or write) cycle, and explanation thereof is omitted. Since the refresh cycle does not need the column address, the chip select signal $\overline{CS}$ is made high before the clock signal CLK rises at t_2 so as to retain the high input signal $\overline{CS}$ to the latch **81**. After the clock signal CLK has risen at t_2, output signal $\overline{CCS}$ of the latch **81** goes high, causing the inverter **11** to have a low inverting output signal CCS. Consequently, the low input signal CCS to the three-output AND gate **15** causes it to produce a column address set signal CS1 at a low level.

In the cycle of t_3, the input signal CCS common to the two-input AND gate **14** and three-input AND gate **15** is low, and therefore the row address set signal RS1 and column address set signal CS1 are low. The operation of the t_4 cycle is identical to that of t_1 in FIG. **4** and explanation thereof is omitted.

In this manner, a row address in the address signal **A0–A9** is introduced to the row latch **2** and no column address is introduced for the refresh cycle.

FIG. **6** shows the page mode read (or write) cycle. The cycle of t_1 operates identically to that of t_1 in FIG. **4**, in which a row address in the address signal **A0–A9** is intro-